Lab 7 – Characterizing CMOS Inverter

CE-3101/021 Digital Elex. and Comp. Interfacing

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**Abstract:**

The ability to rapidly simulate circuits and make changes on the fly is an invaluable tool that has allowed us to analyze circuits rapidly and effectively. This is because of programs like Waveform and the Analog Discovery Kit which allow us to create circuits on a breadboard and then analyze their behavior on a computer. In this lab we are building five different types of inverter circuits. These inverter circuits are made using different transistors such as the RTL, DTL, TTL, PMOS, and CMOS. These circuits were used throughout the years as each model became slightly better than the previous model and improved upon certain aspects. We first simulated each of the circuits by building them in LTSpice to see what the expected output values were and see how each inverter behaved. Then we went ahead and built them on a breadboard and using the Analog Discovery kit and the Waveforms program we were able to view what the actual output values were and see how each inverter functioned.

**Methods:**

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Figure 1: Circuit diagram, taken from Ms.Varnell’s CE3101 Lab 5 document

The circuit in figure 1 show the general layout of how we will be setting up each inverter circuit to be tested with the Analog Discovery Kit and the Waveforms program. The connections to the two channels shall remain the same throughout each circuit and the only difference will be the implementation of which inverter we use. Since there are five inverters this process will be repeated five times. The first inverter we built and tested was the RTL inverter circuit (figure 2), and we went ahead and found the points where the slope was negative one in order to determine the voltage output high (VOH), the voltage output low (VOL), the voltage input high (VIH), the voltage input low (VIL), and the voltage where both meet (VM). Since the slope is negative one on two points in the waveforms, we are able to determine these values, and we look at the intersection for VM. We then repeated this same process for tall of the other inverter circuits (figures 3-6).

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Figure 2: RTL inverter circuit taken from Ms.Varnell's Lab 5 document

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Figure 3: DTL inverter circuit taken from Ms.Varnell's Lab 5 document

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Figure 4: TTL inverter circuit taken from Ms.Varnell's Lab 5 document

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Figure 5: PMOS inverter circuit taken from Ms.Varnell's Lab 5 document

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Figure 6: CMOS inverter circuit taken from Ms.Varnell's Lab 5 document

**Results:**

After conducting the lab, we are able to compare how input and output voltage values between each of the inverter circuits, not only against themselves, but also against the simulated LTSpice values for the same circuit. The two resulting data sets were put into tables that are present in figures 6 and 7. Also, the waveforms graphs from the experiment (figures 8-12) are shown below in order to provide a visual representation of the results of each inverter circuit. The goal for these circuits is to create a point that is a near vertical drop when the output voltage is plotted against the input voltage. Since it is physically impossible for the resulting voltage values to mirror a perfect unit step function we attempt to get as close as possible while also taking into consideration size, efficiency in power, speed, and production cost.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **RTL** | **DTL** | **TTL** | **PMOS** | **CMOS** |
| **VOH** | 4.97V | 4.92V | 4.97V | -146mV | 4.53V |
| **VIL** | 570mV | 200mV | 552mV | -2.98V | 1.99V |
| **VM** | 744mV | 500mV | 684mV | -2.49V | 2.45V |
| **VIH** | 780mV | 540mV | 705mV | -2.64V | 2.91V |
| **VOL** | 136mV | 121mV | 44.7mV | -4.68V | 465mV |
| **NMH** | 4.19V | 4.38V | 4.27V | -2.49V | 1.62V |
| **NML** | 434mV | 80.5mV | 507mV | 1.70V | 1.53V |

Figure 7: Table from the LTSpice simulation of the inverter circuits

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **RTL** | **DTL** | **TTL** | **PMOS** | **CMOS** |
| **VOH** | 4.95V | 4.91V | 4.95V | -133mV | 4.95V |
| **VIL** | 513mV | 132mV | 507mV | -3.19V | 2.00V |
| **VM (Ranged)** | (685-748)mV | (457-558)mV | (652-948)mV | -3.05V | (2.02-2.06)V |
| **VIH** | 714mV | 453mV | 659mV | -2.84V | 2.03V |
| **VOL** | 57.2mV | 66.4mV | 51.0mV | -4.88V | 825mV |
| **NMH** | 4.24V | 4.46V | 4.29V | 2.71V | 2.92V |
| **NML** | 456mV | 65.6mV | 456mV | 1.69V | 1.18V |

Figure 8: Table from the gathered data of the experiment conducted in Waveforms

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Figure 9: RTL experiment waveform

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Figure 10: DTL experiment waveform

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Figure 11: TTL experiment waveform

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Figure 12: PMOS experiment waveform

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Figure 13: CMOS experiment waveform

Each of these waveforms depicts how each inverter behaves and the tables in figures 7 and 8 convey the resulting values voltage input and output at the high and low points. The value for VM is when the voltage input is equal to the voltage output and because of the functionality of the waveforms program the best we can get is a range since we can’t select the exact point in which they are equal, unlike the simulation. The last two rows in these tables are the values for the noise margin high (NMH) and noise margin low (NML). These are the two key sets of data we need to look at when examining our experimental results versus our simulated results. This is because these two values represent the difference between the voltage highs and the difference between the voltage lows respectively. Since the experimental values for the VIH, VIL, VOH, and VOL are not identical to the simulated value because of real-world errors such as the component values not being exact to the tee, we can look at the NMH and NML to see how accurate the experimental results and simulated results are. This is because the real-world error applies throughout the low, high, input, and output values meaning that their differences should still match our simulated results. Now when we look at the results of NMH and NML for the experimental and simulated data we can see that they are almost identical for every case meaning that our experimental data and our simulated data line up.

Now the lab also posed some questions which need to be answered, and these are:

1. **Comment on each of the inverters, their power usage, and how close they are to the ideal inverter step function.**

The first inverter that was designed and built was the RTL inverter and it had a relatively simple design which was a huge advantage; however, it was relatively slow, it contained resistors, so it wasn’t too small, and their needed to be an input current. Next came the DTL which had a better noise margin than the RTL but appeared to be less like the unit step function and suffered from the same issue of being slow and containing resistors. Then came the TTL which improved on the DTL because it was faster and looked more like a unit step function; however, it still contained resistors and required static power. After that came the PMOS which needed no input current and came in a smaller size than the previous inverters; however, it still contained resistors, needed static power, operated at negative voltages, and looked less like the desired unit step function. Lastly there came the CMOS which was small, fast, needed no static power or input current, had no resistors, and it looked very similar to the unit step function. Even though this inverter yielded some of the best results, it still suffered from the fact that it needed two transistors to function and was sensitive to electrostatic discharges. All that being said, the CMOS inverter is the best option because it achieves the desired goal of almost mirroring the unit step function while also being small and fast, and this is the inverter that has been used for years and been constantly refined and improved.

**Summary:**

After conducting this lab and going through all of the data, the most important takeaways are as follows: the behavior of each inverter and how it varies slightly between each iteration, and each iteration attempts to be slightly better than the previous. Currently the CMOS is the most popular and most used because it is the best for its size, speed, requiring no static power, having no resistors, and no input currents. This inverter has been used and refined throughout the years.

**Appendix:**

I provide the SPICE code I wrote that created the simulated inverters and got their data.

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Figure 14: SPICE code for RTL inverter

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Figure 15: SPICE code for DTL inverter

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Figure 16: SPICE code for TTL inverter

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Figure 17: SPICE code for PMOS inverter

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Figure 18: SPICE code for CMOS inverter